Serial No. 09/634,501
Docket No.: NEC00P244-as
WAK.061

AMENDMENTS TO THE CLAIMS:

1-2. (Canceled)

3. (Previously presented) A data processing device, comprising:

a plurality of connection terminals for being individually supplied with signals, including processing data and a clock signal, and drive electric power;

at least one radio antenna for receiving the signals and drive electric power as one radio wave;

a data processing circuit switchable between a terminal mode, in which only the signals supplied to said connection terminals are effective, and an RF mode, in which only the radio wave supplied to said radio antenna is effective, said data processing circuit being supplied with the drive electric power and the signals; and

a mode selecting circuit for setting said data processing circuit to the RF mode by default in response to the drive electric power starting to be supplied, and for switching said data processing circuit to the terminal mode in response to the clock signal being applied to a corresponding one of said connection terminals,

wherein said mode selecting circuit comprises:

clock counting means for counting clock pulses of the clock signal supplied in response to the drive electric power starting to be supplied; and

input deciding means for outputting a switching signal to switch said data processing circuit to said terminal mode when said clock counting means has counted a predetermined number of clock pulses.

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4. (Previously presented) A data processing device according to claim 23, wherein said input deciding means comprises data output means for outputting the reset signal as the switching signal when said clock counting means has counted a predetermined number of clock pulses.

5. (Previously presented) A data processing device according to claim 3, wherein said mode selecting circuit comprises mode maintaining means for applying the switching signal output by said input deciding means as a dummy clock signal to said clock counting means through a feedback loop.

6. (Previously presented) A data processing device according to claim 5, wherein said mode selecting circuit includes a mode maintaining circuit for outputting the switching signal as the dummy clock signal.

7. (Canceled)

8. (Previously presented) A data processing device, comprising:

a plurality of connection terminals for being individually supplied with signals, including processing data and a clock signal, and drive electric power;

at least one radio antenna for receiving the signals and the drive electric power as one radio wave;

PAGE 4/12 * RCVD AT 4/4/2005 6:21:53 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:7037612375 * DURATION (mm-ss):03-50

a data processing circuit switchable between a terminal mode, in which only the signals supplied to said connection terminals are effective, and an RF mode, in which only the radio wave supplied to said radio antenna is effective, said data processing circuit being supplied with the drive electric power and the signals; and

a mode selecting circuit for setting said data processing circuit to the RF mode by default in response to the drive electric power starting to be supplied, and for switching said data processing circuit to the terminal mode in response to the clock signal being applied to a corresponding one of said connection terminals, wherein:

the signals supplied to said connection terminals further include a reset signal;

said mode selecting circuit also switches said data processing circuit to the terminal mode in response to the reset signal being applied to a second corresponding one of said connection terminals, and

said mode selecting circuit comprises:

a clock counter responsive to the initial application of the drive electric power for counting clock pulses of the clock signal supplied to the respective one of said connection terminals; and

said input deciding circuit is responsive to said clock counter counting a predetermined number of clock pulses, for providing the reset signal as the switching signal.

9. (Previously presented) A data processing device according to claim 8, wherein said mode selecting circuit provides the switching signal as a dummy clock signal to said clock counter.

PAGE 5/12 * RCVD AT 4/4/2005 6:21:53 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:7037612375 * DURATION (mm-ss):03-50

10. (Previously presented) A data processing device according to claim 3, further comprising a power extracting circuit for extracting the drive electric power from the radio wave, and a power on clear circuit, responsive to the initial application of the drive electric power, for resetting said clock counter.

11-13. (Canceled)

14. (Previously presented) A data processing device, comprising:

a plurality of connection terminals adapted to be supplied respectively with signals, including processing data and a clock signal, and drive electric power;

at least one radio antenna for receiving processing data and drive electric power in a radio wave;

a data processing circuit switchable between a terminal mode, in which only the signals supplied to said connection terminals are effective, and an RF mode, in which only the radio wave supplied to said radio antenna is effective, said data processing circuit being supplied with the drive electric power and the signals; and

a mode selecting circuit responsive to initial application of the drive electric power to said data processing device for setting said data processing circuit to the RF mode, and further responsive to receipt of the clock signal for applying a switching signal to said data processing circuit to switch said data processing circuit to the terminal mode, wherein said mode selecting circuit comprises:

a clock counter responsive to the initial application of the drive electric power for counting clock pulses of the clock signal supplied to the respective one of said connection terminals; and

an input deciding circuit responsive to said clock counter counting a first predetermined number of clock pulses, for outputting a switching signal to switch said data processing circuit to the terminal mode.

15. (Previously presented) A data processing device according to claim 26, wherein said input deciding circuit is responsive to said clock counter counting a second predetermined number of clock pulses, for providing the reset signal as the switching signal.

16. (Previously presented) A data processing device according to claim 14, wherein said mode selecting circuit provides the switching signal as a dummy clock signal to said clock counter.

17. (Previously presented) A data processing device according to claim 16, wherein said mode selecting circuit includes a mode maintaining circuit for outputting the switching signal as the dummy clock signal.

18. (Previously presented) A data processing device according to claim 14, further comprising a power extracting circuit for extracting the drive electric power from the radio wave, and a power on clear circuit, responsive to the initial application of the drive electric

PAGE 7/12 * RCVD AT 4/4/2005 6:21:53 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:7037612375 * DURATION (mm-ss):03-50

power, for resetting said clock counter.

19. (Canceled)

20. (Previously presented) A data processing device, comprising:

a plurality of connection terminals adapted to be supplied respectively with signals, including processing data and a clock signal, and drive electric power;

at least one radio antenna for receiving processing data and drive electric power in a radio wave;

a data processing circuit switchable between a terminal mode, in which only the signals supplied to said connection terminals are effective, and an RF mode, in which only the radio wave supplied to said radio antenna is effective, said data processing circuit being supplied with the drive electric power and the signals; and

a mode selecting circuit responsive to initial application of the drive electric power to said data processing device for setting said data processing circuit to the RF mode, and further responsive to receipt of the clock signal indicating elapsing of a predetermined period of time for applying a switching signal to said data processing circuit to switch said data processing circuit to the terminal mode, wherein:

the signals supplied to said connection terminals further include a reset signal;

said mode selecting circuit also switches said data processing circuit to the terminal mode in response to the reset signal being applied to a second corresponding one of said connection terminals, and

PAGE 8/12 * RCVD AT 4/4/2005 6:21:53 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:7037612375 * DURATION (mm-ss):03-50

said mode selecting circuit comprises:

a clock counter responsive to the initial application of the drive electric power for counting clock pulses of the clock signal supplied to the respective one of said connection terminals; and

said input deciding circuit is responsive to said clock counter counting a second predetermined number of clock pulses, for providing the reset signal as the switching signal.

21. (Previously presented) A data processing device according to claim 14, wherein said mode selecting circuit provides the switching signal as a dummy clock signal to said clock counter.

22. (Canceled)

23. (Previously presented) A data processing device according to claim 3, wherein:

the signals supplied to said connection terminals further include a reset signal; and

said mode selecting circuit also switches said data processing circuit to the terminal mode in response to the reset signal being applied to a second corresponding one of said connection terminals.

24-25. (Canceled)

PAGE 9/12 * RCVD AT 4/4/2005 6:21:53 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:7037612375 * DURATION (mm-ss):03-50

26. (Previously presented) A data processing device according to claim 14, wherein:

the signals supplied to said connection terminals further include a reset signal; and

said mode selecting circuit also switches to the terminal mode in response to the reset signal being applied to a second corresponding one of said connection terminals.

PAGE 10/12 * RCVD AT 4/4/2005 6:21:53 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:7037612375 * DURATION (mm-ss):03-50

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